Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A universal memory device comprising:

a plurality of interfaces in communication with different external memory clients or communicating according to different memory uses;

a memory including a plurality of low-latency, rewritable, non-volatile memory cells;

a profile storage unit connected to the memory and including access information allocated to at least one request profile, said request profile including at least one set of request information elements and said access information indicating whether an access request, which fits a particular request profile, is to be allowed or rejected;

an access control unit connected with said plurality of interfaces, said profile storage unit, and said memory, said access control unit configured to ascertain a request profile to an access request using request information of said access request, said access control unit further configured to determine access rights of said access request in dependence on the access information allocated to the request profile of the access request;

wherein the plurality of interfaces are functional units each providing specific access characteristics by allocating a set of request profiles to each interface.

2. (currently amended) The universal memory device of claim 1, wherein ~~said request profile includes at least one set of request information elements,~~ said set of request information elements ~~including~~ includes at least one request information element indicating at least one of: a type of request, an external memory client from which the request originates, a memory section the request is directed to, an access authorization, a password, a request protocol type, a time of request, an interface receiving the request,

the length of the request, time span lapsed since a last request, a security class, or a priority class.

3. (canceled)

4. (currently amended) The universal memory device of claim 1~~3~~, wherein at least one of said interfaces is implemented in the form of hardware.

5. (currently amended) The universal memory device of claim 1~~3~~, wherein at least one of said interfaces is implemented in the form of software.

6. (currently amended) The universal memory device of claim 4, further comprising an SRAM-type interface adapted to serve separate connections for address data input and user data exchange, respectively, between the memory device and at least one external memory client.

7. (currently amended) The universal memory device of claim 5, further comprising an I/O-type interface adapted to serve a shared connection for address data input and user data exchange between the memory device and at least one external memory client.

8. (currently amended) The universal memory device of claim 1, further comprising a supervisor interface adapted to create or change at least one request profile and/or access information allocated thereto, given a predetermined condition.

9. (currently amended) The universal memory device of claim 8, wherein said supervisor interface is adapted to admit or reject external requests for change of a request profile, depending on access information allocated to at least one predetermined change request profile.

10. (currently amended) The universal memory device of claim 3, wherein said profile storage unit comprises a set of access flags, each access flag allocated to a respective

request profile, and wherein said access information is given by one of two possible states of an access flag.

11. (currently amended) The universal memory device of claim 1, wherein said profile storage unit is integrated into said access control unit.

12. (currently amended) The universal memory device of claim 1, wherein said access control unit is adapted to maintain a current copy of said profile storage unit in a predetermined section of said memory.

13. (currently amended) The universal memory device of claim 1, further comprising a translation unit adapted to translate between one or more different ways of memory addressing.

14. (canceled)

15. (new) A memory device comprising:

an interface for receiving access requests;

a memory cell array having a plurality of low-latency, rewritable, non-volatile memory cells forming at least one memory section;

a word-select unit connected between the interface and the memory cell array to provide column selection;

a section-select unit connected between the interface and the memory cell array to provide row selection;

a profile storage unit connected to said interface comprising a plurality of request profiles that each represent a profile of an access request, wherein each request profile includes:

a set of request information elements, wherein at least one of the request information elements indicates whether an access request is a read request or a write request; and

an access flag whose state indicates whether a corresponding access request is allowed to access the memory or not allowed to access the memory;

an access control unit connected to said profile storage unit and said memory and configured to allow or reject an access request;

wherein said profile storage unit selects an access flag that corresponds to a request profile in response to an access request that fits the request profile; and

wherein the access control unit allows or rejects an access request in response to the access flag that is selected by the profile storage unit.

16. (new) The memory device of claim 15 wherein the profile storage unit comprises a set of access flags, one access flag for each row address, such that each access flag governs the access to one row of the memory cell array.

17. (new) The memory device of claim 16 wherein the access flags are fast read-out state registers.

18. (new) The memory device of claim 15 wherein the access control unit operates in a data path to admit or reject a flow of data to or from the memory cell array depending on the state of the corresponding access flag it receives from the profile storage unit.

19. (new) The memory device of claim 15 further comprising a memory mapped interface and an I/O mapped interface connected to provide access to the memory cell array.

20. (new) The memory device of claim 19 wherein pins of the memory device are shared by the memory mapped and I/O mapped interfaces.